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(54) **Method for forming coplanar conductor/insulator films.**

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Description

The invention relates to a method for producing coplanar conductor/insulator films with at least one level of metallization on a substrate including the steps of forming on said substrate a conductive pattern having on its top surface a coating consisting of a material being preferably etchable in comparison to the conductor material, blanket depositing a layer of dielectric material whose thickness equals that of the conductive pattern, and wet etching said coating of the preferably etchable material for removal thereof together with the overlying portion of said dielectric material.

Lift-off techniques are finding increased interest and use in the fabrication of integrated circuits to achieve greater component density particularly in large scale integrated circuitry. Typical of the lift-off techniques are those described in US Patents No. 2,559,389, No. 3,849,136, No. 3,873,361 and No. 3,985,597.

One of the patents of particular interest is US 3,985,597 which describes a process for forming an embedded interconnection system on a substrate by forming a first layer of an organic thermosetting polymerized resin layer (such as a polyimide) over the substrate; forming a second overlying layer of a material (such as a polysulfone) that is soluble in a solvent specific to it without appreciably affecting the material of the first layer (e.g. polyimide); forming a third thin barrier layer (e.g. SiO_x, glass resin, etc.) resistive to ion etching in O_2 on the second layer; depositing a resist layer; exposing the resist in a pattern of the desired metallurgy pattern; developing the resist to form a mask of the desired metallurgy pattern; reactive ion etching the resultant exposed areas of the first, second, and third layers; blanket depositing a conductive metal layer having a thickness approximately matching the thickness of the first layer (e.g. polyimide); and exposing the substrate to a solvent that is selective to the material of the second layer (e.g. polysulfone), which is removed together with the overlying portions of the barrier and metal layers.

In contrast to the above US Patent No. 3,985,597, which forms a conductive metal pattern within corresponding recessed openings or grooves of an insulating layer (e.g. polyimide), a particularly unique modification of the process is that of US Patents No. 4,035,276 and No. 4,090,006 in which an insulating layer (e.g. silicon dioxide, glass, etc.) is deposited to embed a preformed conductor pattern coated by a release layer, where the release layer coated conductor pattern is formed by lift-off techniques. The release layer (e.g. copper, chrome, etc.) and the overlying insulator layer are subsequently removed by exposure to an etchant such as concentrated nitric acid. Although the method described in these two US Patents are effective they are still rather complicated and the deviation from planarity is not satisfactory. Another problem is the registration in the subsequent E-beam exposure step since it is difficult to distinguish adequately between aluminum based metallization and silicon dioxide or glass insulators which only have about 100 nm step between them. Also during the etching of the release layer pitting of the surface of the aluminum based metallization occurs.

These drawbacks become more significant in view of the substantial increases in densities of semiconductor devices, particularly with increasing levels of metallization. Such higher densities of the devices render them sensitive to fabrication tolerances. For example, four levels of metallization are becoming common in integrated circuit designs. Even with three levels of metallization, the integrated circuits become wire limited as the density of the device increases. A simpler and improved planar process is also necessary in order to maintain and insure good coverage of metal and insulators at all levels.

It is the object of the invention to provide a simple method for fabricating coplanar conductor/insulator films which have an excellent planarity, and at which the registration for the next E-beam exposure step is facilitated in comparison with known structures, where using said method the surface of the conductive pattern is not attacked when the release layer is removed.

This object is achieved by a method as defined at the beginning of this specification using the features of the characterizing part of claim 1.

The magnesium oxide is used as release layer and also as etch mask in some embodiments of the invention. Very well adapted to the magnesium oxide is the hafnium coating which protects the aluminum based metallization during the removal of the magnesium oxide. The hafnium coating also serves as per registration enhancer for subsequent electron beam steps.

The inventive method is preferably used in forming coplanar conductor/insulator films on components such as integrated circuits or dielectric substrates employed in the fabrication and packaging of semiconductor components.

With the inventive method, structures with interconnected coplanar conductor/insulator films on different levels are preferably produced on a substrate.

Other advantageous embodiments of the inventive method are disclosed in the subclaims.

The invention will become more apparent from the following detailed description taken in conjunction with the accompanying drawings.

In the drawings forming a material part of this disclosure:

Figs. 1A to 1G are diagrammatic cross-sectional views illustrating a substrate at various stages of fabrication in accordance with one embodiment of the concept of the invention described herein.

Figs. 2A to 2I show a sequence of elevational views, in broken section, illustrating a substrate at various stages of fabrication in accordance with another embodiment of the concept of the invention described herein.

Figs. 3A to 3H also show a sequence of eleva-

tional views, in cross-section, illustrating the fabrication of structure in accordance with a further embodiment of the concept of the invention described herein.

Figs. 4A to 4G are schematic cross-sectional views illustrating the fabrication of multi-level metallization from preformed first level insulator/metallization obtained by the processing of Figs. 1A to 1G, 2A to 2H and 3A to 3H, utilizing the concept of the invention described herein.

It has been found in accordance with this invention that protectively coating a conductor pattern, on a dielectric substrate, with a film of hafnium, in conjunction with a dry etch mask of MgO as described in US Patent 4,132,586, simplifies the fabrication process for planar insulator/conductor structure with enhanced protection of the conductor pattern, and which also enables enhanced registration capabilities for any following E-beam processing.

As shown in the embodiment of Figs. 2A to 2I for example, for purposes of fabricating semiconductor devices, a blanket layer of a conductive metal (e.g. an aluminum based metal, such as aluminum, aluminum-copper alloy, etc.) is deposited, as by evaporation or sputtering, over an integrated circuit structure, including any insulating layers thereon, such as silicon dioxide, Si_3N_4, or composites thereof, glass, and the like. This is followed by blanket deposition of a film of hafnium, by any conventional manner (e.g. evaporation or sputtering) over the aluminum layer.

A lift-off mask is then formed over the hafnium layer defining a pattern of openings corresponding to the desired conductor pattern. This lift-off mask can be formed by well known techniques which can be found described in the above noted patents, as well as in US Patents No. 3,421,206, No. 3,934,057, No. 3,982,943 and No. 4,004,044.

Illustratively, in accordance with these lift-off techniques, a polysulfone lift-off layer can be applied by spin-coating, which is then cured on a hotplate. A barrier layer of SiO_x (or glass resin) is then deposited by evaporation, spinning or PECVD (plasma enhanced chemical vapor deposition), as appropriate, over the lift-off layer. This is followed by coating the structure with an appropriate resist followed by exposure and development using standard photo or electron-beam lithographic techniques to form a pattern of openings corresponding to the desired conductor pattern.

Using the patterned resist as a masking layer, conformal openings can be suitably formed in the barrier layer, as for example by RIE utilizing any suitable ambient, which for a silicon monoxide barrier layer can comprise a carbon tetrafluoride (CF_4) ambient.

This is normally followed by suitable etching of conformal openings in the polymer (e.g. polysulfone) sub-base of the lift-off structure, as for example, again by RIE in the same sputtering chamber in which, for a polysulfone base, the ambient can be switched, with purging, to an oxygen containing atmosphere to which silicon monoxide is comparatively resistant. As will be appreciated, the provision of the indicated conformal openings in the lift-off mask exposes a corresponding pattern of the composite hafnium/aluminum films. The resist here is removed coincidently by the O_2-RIE etching of the "polysulfone layer".

A blanket layer of magnesium oxide (MgO) is then deposited, as by evaporation, over the lift-off mask and the exposed portions of the compositely layered metallization, followed by removal of the lift-off mask by solvation of the lift-off polymer in a suitable solvent, such as n-methyl pyrrolidinone (NMP) at 60°C for polysulfone. On removal of the lift-off mask with its overlying barrier layer and magnesium oxide layer, a dry etch mask of magnesium oxide is retained to expose complementary portions of the hafnium/aluminum composite metallization. Further details of the formation of the MgO dry etch mask can be obtained by reference to US Patent 4,132,586.

The MgO masked structure is then subjected to dry etching processes for removal of the exposed portion of the hafnium/aluminum composite. For example, for a hafnium coated aluminum-copper alloy composite the dry etching can be effected by RIE at 0.4 watts per cm^2 at 13.56 MHz in a CCl_4/argon plasma in accordance with the system described in US Patent No. 3,994,793.

In the operation, an insulator (such as glass, SiO_2, etc.) is blanket deposited by rf sputtering, to cover the exposed substrate, and the MgO mask. Normally, the insulator will be deposited to a level matching the thickness of the composite metal conductor pattern.

The insulator may be sputter deposited under conditions which cause considerable resputtering at the substrate. This causes the sidewalls of the MgO mask to be substantially free of deposited insulator after completion of the insulator deposition. Alternately, the insulator may be sputter deposited under conditions which effect lower resputtering at the substrate. Any insulator deposited on the sidewalls of the MgO mask may then be removed by increasing the resputtering at the substrate. The resputtering can be adjusted so that only the excess insulator on the sidewalls of the MgO is removed without appreciably changing the thickness of the insulator deposited to cover the exposed substrate. Another method of deposition of the insulator is to blanket sputter deposit the insulator to a level in excess of the thickness of the composite metal conductor pattern and then to remove the excess insulator by rf sputter etching. The etch-back step causes the sidewalls of the MgO mask to be free of deposited insulator.

The basic processing concept is completed by removal of the MgO mask, and the overlying portions, by exposure to a suitable solvent such as solution of oxalic acid, ammonia oxalate, acetic acid, phosphoric acid/chromic acid, and the like.

Although the above describes the formation of

a single level of a coplanar conductor/insulator pattern, the invention is also comprehended for use in forming multi-level structures. In particular, the invention is also intended for the formation of via studs, interconnections, or feedthroughs between metallization levels using the same basic step.

Also, although the invention described above has been with respect to its application for forming semiconductor devices, the invention is equally applicable to the formation of metallization patterns on a dielectric module (e.g. ceramics, as alumina, glass, glass-ceramics, etc.) such as described in US Patents No. 3,726,002, No. 3,968,193, No. 4,221,047 and No. 4,234,367, which are employed for supporting integrated circuit chips or devices and appropriate associated circuitry.

However applied, the critical parts of the invention reside in the described use of hafnium and magnesium oxide in view of their coordinated unique functions.

The MgO layer forms a suitable lift-off layer for SiO_2 deposition because it withstands the relatively high temperatures of SiO_2 sputter deposition. Also, it likewise has a very low erosion rate for reactive ion etching in CCl_4, and therefore can serve as an RIE mask to form the metal patterns.

Hafnium serves as a protective layer for the metallization (e.g., aluminum/copper alloy) during the etch of the MgO lift-off mask in etchants (e.g. phosphoric acid/chromic acid mix). For example, above 40°C the phosphoric/chromic acid etch attacks aluminum/copper alloys and causes pitting of the metal. However, with a protective layer of hafnium, etching of the MgO mask in the phosphoric/chromic etch at 80°C can be accomplished without attack of the aluminum/copper alloy. As a result, this allows the MgO lift-off to proceed at a much faster rate than if the etch temperature were limited to less than 40°C. A typical rate employing the protective hafnium coating at 80°C enables the lift-off of a 0.254 mm wide MgO pattern in 10 minutes.

Also the use of the hafnium was found to be a registration enhancer for subsequent E-beam exposure processes. The presence of the hafnium over, for example, aluminum/copper alloys enables E-beam exposure units to register to the metal pattern. Without Hf, it is very difficult to adequately distinguish between the metal and insulator (e.g. SiO_2) because there is only about a 100 nm step between the two.

Referring to the drawings, and to Figs. 1A to 1G in particular, there is shown a substrate 1 which is typically monocrystalline silicon or other semiconductor material, with an overlying layer 2 of a dielectric coating, as for example SiO_2, Si_3N_4, or composites thereof, and the like. The substrate 1 in this embodiment of the invention is comprehended as an integrated circuit device having active and passive devices fabricated therein (not shown) and means for electrically isolating the devices from each other. In such application, the insulating layer 2 is normally provided with contact openings (not shown) for making contact to the active and passive devices. However, the substrate can also be a body of insulating material when the process is used to form metallurgy patterns on a dielectric module (e.g., alumina ceramics, glass-ceramics, etc.) for supporting integrated circuit chips or devices, and appropriate associated circuitry.

Next a layer 3 of lift-off masking material is coated over the insulating layer 2. This masking material is characterized as an organic polymer material, such as described in the above noted patents, or standard photo or electron beam resists which can be applied in any conventional manner, as by spin coating. Where resists are employed, they can be processed into a lift-off mask with a pattern of openings 4 by exposure and development in accordance with conventional lithographic techniques well known in the integrated circuit fabrication art.

Where the desired metallization of the following step is to be a first level conductive pattern, the opening pattern 4, of the mask, will include extensions in registration with the contact openings to active devices of an integrated circuit substrate through the insulator layer 2.

As indicated, other polymeric materials can be employed in forming the lift-off mask 3. For example, these materials can comprise polysulfones, polycarbonates, heat-stabilized Shipley AZ-1350J resist (a cresol formaldehyde containing an o-quinonediazide sensitizer) etc. which can be suitably deposited for layer 3. It is only necessary that the material chosen be such that it is soluble in a solvent selective to it. One effective material is a polysulfone polymerized resin formed by reacting sulfur dioxide with aromatic or alphatic vinyl compounds. A typical polysulfone is sold under the trademark ICI 100-P by Imperial Chemical Inc. The polysulfone is available as a relatively viscous liquid which can be deposited on a substrate, e.g. semiconductor wafer, and then spun in the range of 4000 rpm. Preferably, the polysulfone material, which is in a solution of n-methyl pyrrolidinone, is deposited and spun in a low humidity air or in N_2 atmosphere. The material is subsequently cured by heating for five minutes at 80°C and for 20 minutes at 300°C.

A relatively thin barrier film (not shown) is normally deposited over the polysulfone material where the structure is to be subjected to reactive ion etching in O_2 (as in other embodiments of this invention). This barrier film can be a layer of SiO_2, SiO_x, Al_2O_3, Si, $Si_xN_yH_z$, glass resin or a metal layer, as in US Patents No. 4,035,276 and No. 4,090,006. A typical material for the barrier layer is SiO_x deposited by evaporation or plasma enhanced chemical vapour deposition (PECVD). However, any suitable type of glass or inorganic material that is resistant to reactive ion etching, particularly in an ambient of O_2 or an ambient that contains O_2, can be used. A layer of a photo or an E-beam resist is then deposited over the structure, exposed in the desired conductor pattern,

and developed in accordance with known lithographic technology. One preferred method of forming conformal openings in the lift-off mask, through the resist mask, is by reactive ion etching, where the substrate is exposed to a reactive ion plasma generated in an appropriate ambient by an rf source in a sputter apparatus such as described in US Patent No. 3,498,710. In removing the material, in the case where it is a SiO_x, the ambient at least includes CF_4. Subsequently, the ambient in the sputter apparatus is changed to an O_2 ambient and the exposed portions of sub-layer of the lift-off mask structure, e.g. polysulfone, is removed. For purpose of this application such a composite SiO_x/polysulfone lift-off mask is comprehended as equivalent to the resist mask 3 of the drawings, with the term "lift-off mask" in turn comprehending all equivalent lift-off mask structures.

Next, as shown in Fig. 1B, a layer 5 of a functional conductive metal (e.g. aluminum, aluminum-copper alloys, and the like) is blanket deposited, as by evaporation or sputtering over the surface of the structure, resulting in a metal layer on top of the lift-off mask and on the portions of the substrate exposed by the openings 4 in the lift-off mask 3. As shown in Fig. 1C, a layer 6 of hafnium is blanket deposited over the structure, which encompasses the metallization 5 on lift-off mask 3 and in the openings thereof, followed by blanket deposition of magnesium oxide layer 7 over the structure as shown in Fig. 1D.

In the next operation, as shown in Fig. 1E, the lift-off mask and all overlying layers are then removed by exposing the substrate to a solvent specific for the lift-off masks. In the case of polysulfones, the solvent is n-methyl pyrrolidinone at 60°C enhanced by ultrasonic agitation. As shown the resultant structure forms a composite pattern 8 of deposited segments 5A, 6A and 7A.

With the composite pattern 8 in place, an insulator 9 is deposited in blanket fashion over the structure as shown in Fig. 1F to a thickness substantially that of the composite hafnium/metal segments 5A and 6A. In the preferred form, the insulator can be SiO_2, glass and the like, which can be deposited by rf sputtering. The rf sputter deposition of the insulator may be made under conditions which cause considerable resputtering at the substrate. This causes the sidewalls of the MgO mask to be substantially free of deposited insulator after completion of the insulator deposition. Alternately, the insulator may be sputter deposited under conditions which effect lower resputtering at the substrate. Any insulator deposited on the sidewalls of the MgO mask may then be removed by increasing the resputtering at the substrate. The resputtering can be adjusted so that only the excess insulator on the sidewalls of the MgO is removed without appreciably changing the thickness of the insulator deposited to cover the exposed substrate. Another method of deposition of the insulator is to blanket sputter deposit the insulator to a level in excess of the thickness of the composite metal conductor pattern and then to remove the excess insulator by rf sputter etching. The etch-back step causes the sidewalls of the MgO mask to be free of deposited insulator.

In the next operation, the magnesium oxide segment 7A of composite pattern 8 together with the overlying insulator, is removed or lifted off in a suitable solvent or etchant, as for example, a phosphoric/chromic acid mix among those noted above. The resultant structure is shown in Fig. 1G which may illustratively comprise a first level conductive pattern of a multi-level metallization.

Figs. 2A to 2I representative of modification of the concept of the invention to another embodiment. As above, the structure illustrated is shown with a coating of an insulator 2, e.g. SiO_2, over a substrate 1, such as a semiconductor device or a ceramic substrate. The insulation 2 is then coated sequentially with a metallization layer 5 (Fig. 2A, e.g. aluminum-copper alloy), and a hafnium layer 6 (Fig. 2B). In the next step a lift-off mask 3 is formed over the composite metallization 5 and 6, followed by blanket deposition of a magnesium oxide layer 7. After removal of the lift-off mask 3, together with the overlying MgO portions, the resultant structure is shown in Fig. 2E where the retained MgO segment 7A forms a dry etch mask comparable to that described in US Patent 4,132,586.

The magnesium oxide masked structure is then subjected to dry etching for removal of the exposed portions of the composite hafnium/conductor films 6/5 down to the insulator 2. For example, with the exposed composite metal films 6/5 comprised of hafnium and aluminum-copper alloy, it can be dry etched by reactive ion etching through the hafnium and the aluminum-copper alloy in a CCl_4/argon ambient, in the manner sequentially shown in Figs. 2E and 2F to that of Fig. 2G.

An insulator 9, such as SiO_2 or glass for example, is then blanket deposited as above, over the structure, followed by lift-off removal of the MgO segment 7A and the overlying segment of the insulator by use of suitable solvents. The resultant structure shown in Fig. 2I is equivalent to that of Fig. 1G, each characterized with a coplanar insulator/conductor surface.

Figs. 3A to 3H illustrate a variation of the preceding embodiment in which a lift-off mask 3 is formed on an aluminum film, followed by blanket depositions of a hafnium layer 6 and a MgO layer 7, which on removal of the lift-off mask 3 form a dry etch mask of MgO and Hf segments 7A and 6A. On reactive ion etching of the exposed portions of the metallization 5, the resultant structure shown in Fig. 3F is comparable to that of Fig. 2G, with subsequent processing being the same as that through Figs. 2G to 2I to produce the resultant structure of Fig. 3H which is equivalent to that of Figs. 1G and 2I.

Although the process has been discussed with reference to formation of a single level of coplanar insulator/conductor structures, it is also

effective in forming multi-level structures. Specifically, the formation of via studs or interconnecting feed-throughs between spaced levels of metallization is also comprehended. The formation of a typical interconnecting stud is shown in Figs. 4A to 4F. Shown in Fig. 4A is substrate 1 with a single level conductor formed in accordance with this invention to correspond to those of Figs. 1G, 2I and 3H. As above, the formation of vertical interconnecting stud employs the use of a lift-off mask 3A illustratively formed with an opening 10 over a selected segment 5B/6B of the first level conductor pattern 5A/6A.

In Fig. 4C, a functional conductive metal layer 11 overcoated with a hafnium layer 12 is blanket coated over the substrate, as discussed above. This is followed with a blanket overcoating of a magnesium oxide layer 13, followed by removal of the lift-off mask 3A leaving a mesa or stud of the functional metal segment 11A and the hafnium segment 12A, and the MgO segment or cap 13A as shown in Fig. 4D. Again, aluminum based metals, including aluminum and aluminum-copper alloy are illustratively comprehended in view of their highly reactive properties.

An insulator layer 14 (as of SiO_2, glass, etc.) is then blanket deposited over the substrate, inclusive of the MgO cap 13A to a thickness substantially that of the combined thickness of the functional metal/hafnium segments 11A/12A.

As shown in Fig. 4F, the process for forming the interconnecting feedthrough stud is completed by lifting off the MgO cap 13A together with the overlying portion of the insulating layer 14 in a suitable etchant as described above. As will be appreciated where the same insulator, e.g. SiO_2, is employed in all stages of fabrication, the original insulation 2, and deposited layers 9 and 14 will be integrated into a unitized insulator composite 15 (as shown in Figs. 4E and 4F).

Fig. 4G illustrates a five level conductor structure formed atop a substrate using the same process steps to achieve the three levels of metallization as well as the interconnecting studs between levels. Thus, the metallization composites, of the function metal and hafnium components 5A/6A, 16A/17A and 20A/21A are the conductive patterns formed in three levels with adjacent levels interconnected respectively with interconnecting studs formed of functional metal/hafnium components 11A/12A and 18A/19A.

Thus, as will be apparent to those skilled in the art, any desired number of interconnected layers can be formed by repeating the steps of the various embodiments described above, including intermixing of the basic steps of the embodiments at various metallization and stud levels.

Claims

1. Method for producing coplanar conductor/insulator films with at least one level of metallization on a substrate including the steps of forming on said substrate a conductive pattern having on its top surface a coating consisting of a material being selectively etchable in comparison to the conductor material, blanket depositing a layer of a dielectric material whose thickness equals that of the conductive pattern, and wet etching said coating for removal thereof together with the overlying portions of said dielectric material thereon, characterized in that said pattern is formed of a composite consisting of a lower layer (5A) of an aluminum based metal and an upper layer (6A) of hafnium and that said coating (7) is made of magnesium oxide.

2. Method according to claim 1, wherein said substrate is formed of a passivating coating (2) on a semiconductor device (1) having at least one integrated circuit therein.

3. Method according to claim 2, wherein said coating (2) has at least one via opening for interconnection of an element of said device (1) to said pattern (5A, 6A).

4. Method according to claim 1, wherein said substrate is formed of a ceramic or a glass ceramic.

5. Method according to any one of claims 1 to 4, comprising the steps of

A) forming on said substrate a lift-off mask (3) having a pattern of openings (4) to define a desired conductive pattern,

B) sequentially blanket depositing over said substrate inclusive of said lift-off mask (3) films (5, 6 and 7) of an aluminum based metal, hafnium and magnesium oxide,

C) removing said lift-off mask (3) with the overlying layers of said sequential films (5, 6 and 7) thereon,

D) blanket sputter depositing a layer (9) of a dielectric over said substrate and the pattern formed of the remainder of films (5A, 6A and 7A), and

E) selectively wet etching said magnesium oxide film (7A) for removal thereof and overlying portion of the dielectric layer (9) thereon.

6. Method according to any one of claims 1 to 4, comprising the steps of

A) depositing a first film of an aluminum based metal over said substrate,

B) forming over said first film a lift-off mask having a pattern of openings to define a desired conductive pattern,

C) sequentially blanket depositing over said substrate inclusive of said mask, films of hafnium and magnesium oxide,

D) removing said lift-off mask with the overlying portions of said hafnium and magnesium oxide films,

E) selectively removing the exposed portions of said film of the aluminum based metal by dry etching,

F) blanket depositing a layer of a dielectric over said substrate and the pattern formed by the remainder of said films, and

G) selectively wet etching said mangesium oxide for removal thereof together with overlying portions of the dielectric thereon.

7. Method according to any one of claims 1 to 4, comprising the steps of

A) sequentially blanket depositing a first film (5) of an aluminum based metal and a second film (6) of hafnium over said substrate (2),

B) forming over said second film (6) a lift-off mask (3) having a pattern of openings defining a desired conductive pattern,

C) blanket depositing over said substrate (2), inclusive of said mask (3) and the exposed portions of said second film (6), a layer (7) of magnesium oxide,

D) removing said lift-off mask (3) and portions of said magnesium oxide layer (7) thereon,

E) sequentially removing the exposed portions of said second and first films (5, 6) by dry etching,

F) blanket depositing a layer (9) of a dielectric over said substrate (2) and the pattern formed by the remainder of said films (5, 6) and layer (7A), and

G) selectively etching said magnesium oxide for removal thereof together with overlying portions of the dielectric thereon.

8. Method for forming coplanar conductor/insulator films including a conductive pattern serving as interconnection between two levels of conductors, wherein on a structure as formed according to any one of claims 1 to 7 a pattern formed of a composite consisting of a lower layer (11A) of an aluminum based metal and an upper layer (12A) of hafnium and a magnesium oxide layer (13A) covering the top surface of said pattern are produced according to any one of claims 1 to 7 with said structure being the substrate, wherein a layer (14) of a dielectric is blanket sputtered deposited over said structure and the pattern formed by the remainder of layers (11A, 12A and 13A) where the dielectric layer (14) equals in thickness the combined layer (11A and 12A) and wherein said magnesium oxide layer is wet etched to remove thereof together with overlying portions of dielectric thereon.

9. Method for forming coplanar conductor/insulator films including a conductive pattern serving as a conductor level interconnected with a conductive pattern underneath by using the method according to claim 8, where the structure on which the conductor/insulator films are formed is the one formed according to claim 8.

10. Method for producing a coplanar conductor/insulator structure with several interconnected levels of metallization wherein after the formation of a structure using a method according to any one of claims 1 to 7 the methods of claims 8 and 9 are repeated once or several times.

Patentansprüche

1. Verfahren zum Herstellen koplanarer Leiter/Isolierschichten mit mindestens einer Metallisierungsebene auf einem Substrat einschließlich der Herstellungsschritte:

Herstellen eines auf dem Substrat aufgebrachten Leitungsmusters, auf dessen oberer Oberfläche eine Abdeckung aus einem Material liegt, welches selektiv verglichen mit dem Leitermaterial geätzt werden kann, ganzflächiges Aufbringen einer Schicht aus dieleketrischem Material, deren Stärke gleich der des Leitungsmusters ist, und Naßätzen dieser Schicht, um die zusammen mit den sich darüber befindlichen Teilen des dielektrischen Materials zu entfernen, dadurch gekennzeichnet, daß das Muster aus einem Verbund geformt ist, welcher aus einer unteren Schicht (5A) von auf Aluminium basierendem Metall und einer oberen Schicht (6A) aus Hafnium besteht, und daß diese Abdeckung aus Magnesiumoxid besteht.

2. Verfahren nach Anspruch 1, worin das Substrat von einer Passivierungsschicht (2) auf einer Halbleitervorrichtung (1) mit mindestens einer integrierten Schaltung gebildet wird.

3. Verfahren nach Anspruch 2, worin die schicht (2) mindestens eine Öffnung für die Verbindung eines Elements der Vorrichtung (1) mit dem Muster (5A, 6A) aufweist.

4. Verfahren nach Anspruch 1, worin das Substrat aus Keramik oder Glaskeramik hergestellt ist.

5. Verfahren nach einem der Ansprüche 1 bis 4, folgende Schritte umfassend:

A) Herstellen auf dem Substrat einer Abhebemaske (3) mit einem Muster von Öffnungen (4) zur Definition eines erwünschten Leitungsmusters,

B) sequentielles ganzflächiges Aufbringen über dem Substrat einschließlich der Abhebemaske (3) von Schichten (5, 6, 7) aus einem auf Aluminium basierenden Metall, Hafnium und Magnesiumoxid,

C) Entfernen der Abhebemaske (3) mit den darüberliegenden sequentiellen Schichten (5, 6 und 7),

D) ganzflächiges Aufbringen mittels Kathodenzerstäuber einer dielektrischen Schicht (9) über dem Substrat und dem Muster aus dem Rest der Schichten (5A, 6A und 7A), sowie

E) selektives Naßätzen des Magnesiumoxidfilms (7A) zu dessen Entfernung sowie zur Entfernung des darüberliegenden Teils der dielektrischen Schicht (9).

6. Verfahren nach einem der Ansprüche 1 bis 4, folgende Schritte umfassend:

A) Aufbringen einer ersten Schicht aus auf Aluminium basierendem Metall über dem Substrat,

B) Herstellen einer Abhebemaske über der ersten Schicht mit einem Muster aus Öffnungen zur Definition eines bestimmten Leitungsmusters,

C) sequentielles ganzflächiges Aufbringen über dem Substrat und der Maske eines Films aus Hafnium und Magnesiumoxid;

D) Entfernen der Abhebemaske mit den darüberliegenden Teilen des Hafnium- und Magnesiumoxidfilms,

E) selektives Entfernen der freiliegenden Teile der Schicht aus auf Aluminium basierendem Metall mittels Trockenätzens,

F) ganzflächiges Aufbringen einer dielektrischen Schicht über dem Substrat und dem durch den Rest des verbleibenden Films gebildeten Muster, sowie

G) selektives Naßätzen des Magnesiumoxids zu dessen Entfernung zusammen mit darüberliegenden Teilen der dielektrischen Schicht.

7. Verfahren nach einem der Ansprüche 1 bis 4, folgende Schritte umfassend:

A) sequentielles ganzflächiges Aufbringen einer ersten Schicht (5) aus auf Aluminium basierendem Metall und einer zweiten Schicht (6) aus Hafnium über dem Substrat (2),

B) Herstellen einer Abhebemaske (3) über der zweiten Schicht (6) mit einem ein Leitungsmuster definierenden Muster aus Öffnungen,

C) ganzflächiges Aufbringen einer Magnesiumoxidschicht (7) über dem Substrat (2), der Maske (3) und den frei liegenden Teilen der zweiten Schicht (6),

D) Entfernen der Abhebemaske (3) und von Teilen der sich darauf befindlichen Magnesiumoxidschicht (7),

E) sequentielles Entfernen der frei liegenden Teile der zweiten und ersten Schichten (6) mittels Trockenätzen,

F) ganzflächiges Aufbringen einer Schicht (9) eine dielektrischen Materials über dem Substrat (2) und dem aus dem Rest der Schichten (5, 6) und der Schicht (7A) verbleibenden Muster, sowie

G) selektives Ätzen des Magnesiumoxids zu dessen Entfernung zusammen mit darüberliegenden Teilen des dielektrischen Materials.

8. Verfahren zum Herstellen von koplanaren Leiter/Isolierschichten mit einem Leitungsmuster, welches als Verbindung zwischen zwei Leiterebenen dient, worin auf einer gemäß einem der Ansprüche 1 bis 7 gebildeten Struktur ein Muster aus einem Verbund hergestellt wird, welcher aus einer unteren Schicht (11A) von auf Aluminium basierendem Metall, einer oberen Schicht (12A) aus Hafnium und einer Magnesiumoxidschicht (13A) über der Oberfläche des Musters besteht, gemäß einem der Ansprüche 1 bis 7, wobei die Struktur das Substrat ist, und worin eine Schicht (14) auf einem dielektrischen Material ganzflächig über der Struktur und dem aus dem Rest der Schichten (11A, 12A und 13A) bestehenden Muster ausgebracht wird, wobei die Dicke der dielektrischen Schicht (14) gleich der des Verbunds (11A und 12A) ist, und worin die Magnesiumoxidschicht naßgeätzt wird, um zusammen mit den darüberliegenden Teilen des dielektrischen Materials entfernt zu werden.

9. Verfahren zum Herstellen koplanarer Leiter/Isolierschichten, mit einem Leitungsmuster, welches als Leiterebene in Verbindung mit einem darunterliegenden Leitungsmuster dient, gemäß dem Verfahren nach Anspruch 8, wo die Struktur, auf welcher die Leiter/Isolierschichten ausgebildet werden, diejenige ist, welche gemäß Anspruch 8 hergestellt wurde.

10. Verfahren zum Herstellen einer koplanaren Leiter/Isollerstruktur mit verschiedenen untereinander verbundenden Metallislerungsebene, wo nach der Bildung einer Struktur gemäß dem Verfahren nach einem der Ansprüche 1 bis 7 die Verfahren der Ansprüche 8 und 9 ein oder mehrere Male wiederholt werden.

Revendications

1. Procédé pour former sur un substrat des couches conductrices/isolantes coplanaires comportant au moins un niveau de métallisation, comprenant les opérations suivantes: on forme sur le substrat un motif conducteur portant à sa surface supérieure un revêtement constitué par une matière pouvant être attaquée sélectivement, en comparaison avec la matière conductrice, on effectue un dépôt général d'une couche de matière diélectrique dont l'épaisseur est égale à celle du motif conducteur, et on attaque le revêtement par voie humide pour l'enlever en compagnie des parties de la matière diélectrique qui le recouvrent, caractérisé en ce que le motif précité est formé par une structure composite comprenant une couche inférieure (5A) d'un métal à base d'aluminium et une couche supérieure (6A) de hafnium, et en ce que le revêtement précité (7) est constitué par de l'oxyde de magnésium.

2. Procédé selon la revendication 1, dans lequel le substrat est formé par un revêtement de passivation (2) sur un dispositif à semiconducteur (1) dans lequel se trouve au moins un circuit intégré.

3. Procédé selon la revendication 2, dans lequel le revêtement (2) comporte au moins une ouverture de passage pour l'interconnexion d'un élément du dispositif (1) avec le motif précité (5A, 6A).

4. Procédé selon la revendication 1, dans lequel le substrat est formé par une céramique ou une vitrocéramique.

5. Procédé selon l'une quelconque des revendications 1 à 4, comprenant les opérations suivantes:

A) on forme sur le substrat un masque de décollement (3) comportant un motif d'ouvertures (4) destiné à définir un motif conducteur désiré,

B) on effectue séquentiellement sur le substrat, y compris sur le masque de décollement (3) des dépôt généraux séquentiels de couches (5, 6 et 7) d'un métal à base d'aluminium, de hafnium et d'oxyde de magnésium,

C) on enlève le masque de décollement (3) avec les couches déposées séquentiellement (5, 6 et 7) qui le recouvrent,

D) on effectue un dépôt général, par pulvérisation cathodique, d'une couche (9) d'un diélectrique, sur le substrat et sur le motif formé par la partie restante des couches séquentielles (5A, 6A et 7A), et

E) on attaque sélectivement par voie humide la couche d'oxyde de magnésium (7A), pour enlever cette couche ainsi que la partie de la couche diélectrique (9) qui la recouvre.

6. Procédé selon l'une quelconque des revendications 1 à 4, comprenant les opérations suivantes:

A) on dépose sur le substrat une première couche d'un métal à base d'aluminium,

B) on forme sur cette première couche un

masque de décollement comportant un motif d'ouvertures destiné à définir un motif conducteur désiré,

C) on effectue séquentiellement sur le substrat, y compris sur le masque, des dépôts généraux de couches de hafnium et d'oxyde de magnésium,

D) on enlève le masque de décollement avec les parties des couches de hafnium et d'oxyde de magnésium qui le recouvrent,

E) on enlève sélectivement les parties à nu de la couche de métal à base d'aluminium, par attaque par voie sèche,

F) on effectue un dépôt général d'une couche d'un diélectrique sur le substrat et sur le motif formé par la partie restante des couches déposées séquentiellement, et

G) on attaque sélectivement l'oxyde de magnésium, par voie humide pour l'enlever en compagnie des parties du diélectrique qui le recouvrent.

7. Procédé selon l'une quelconque des revendications 1 à 4, comprenant les opérations suivantes:

A) on effectue séquentiellement des dépôts généraux sur le substrat (2) d'une première couche (5) d'un métal à base d'aluminium et d'une seconde couche (6) de hafnium,

B) on forme sur la seconde couche (6) un masque de décollement (3) comportant un motif d'ouvertures définissant un motif conducteur désiré,

C) on effectue un dépôt général d'une couche (7) d'oxyde de magnésium sur le substrat (2), y compris sur le masque (3) et sur les parties à nu de la seconde couche (6),

D) on enlève le masque de décollement (3) et les parties de la couche d'oxyde de magnésium (7) qui le recouvrent,

E) on enlève séquentiellement les parties à nu des seconde et première couches (5, 6), par attaque par voie sèche,

F) on effectue un dépôt général d'une couche (9) d'un diélectrique, sur le substrat (2) et sur le motif formé par la partie restante des première et seconde couches (5, 6) et de la couche d'oxyde de magnésium (7A), et

G) on attaque sélectivement l'oxyde de magnésium pour l'enlever en compagnie des parties du diélectrique qui le recouvrent.

8. Procédé pour former des couches conductrices/isolantes coplanaires comprenant un motif conducteur faisant fonction d'interconnexion entre deux niveaux de conducteurs, dans lequel, sur une structure formée conformément à l'une quelconque des revendications 1 à 7, on forme un motif composite constitué par une couche inférieure (11A) en un métal à base d'aluminium et par une couche supérieure (12A) en hafnium, et une couche d'oxyde de magnésium (13A) recouvrant la surface supérieure de ce motif, en procédant conformément à l'une quelconque des revendications 1 à 7, avec la structure précitée constituant le substrat, dans lequel on effectue un dépôt général par pulvérisation cathodique d'une couche (14) d'un diélectrique, sur la structure précitée et sur le motif formé par la partie restante des couches (11, 12A et 13A), la couche diélectrique (14) ayant une épaisseur égale à l'épaisseur de la couche combinée (11A et 12A), et dans lequel on attaque la couche d'oxyde de magnésium, par voie humide, pour l'enlever en compagnie des parties de diélectrique qui la recouvrent.

9. Procédé pour former des couches conductrices/isolantes coplanaires comprenant un motif conducteur qui constitue un niveau conducteur interconnecté avec un motif conducteur situé au-dessous de lui, par l'utilisation du procédé conforme à la revendication 8, dans lequel la structure sur laquelle les couches conductrices/isolantes sont formées est celle formée conformément à la revendication 8.

10. Procédé pour produire une structure conductrice/insolante coplanaire avec plusieurs niveaux de métallisation interconnectés, dans lequel, après la formation d'une structure en utilisant un procédé conforme à l'une quelconque des revendications 1 à 7, on répète une ou plusieurs fois les procédés des revendications 8 et 9.

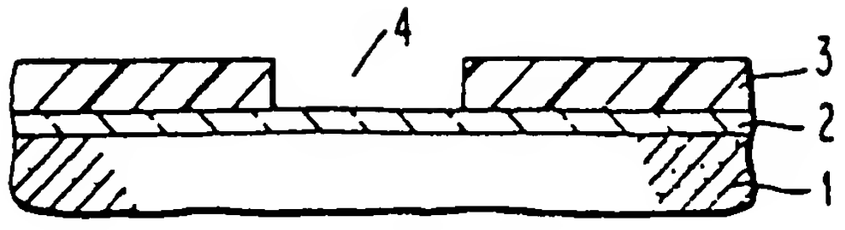

FIG. 1A

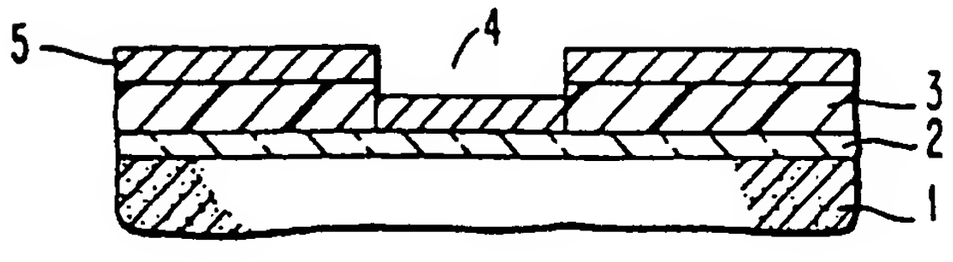

FIG. 1B

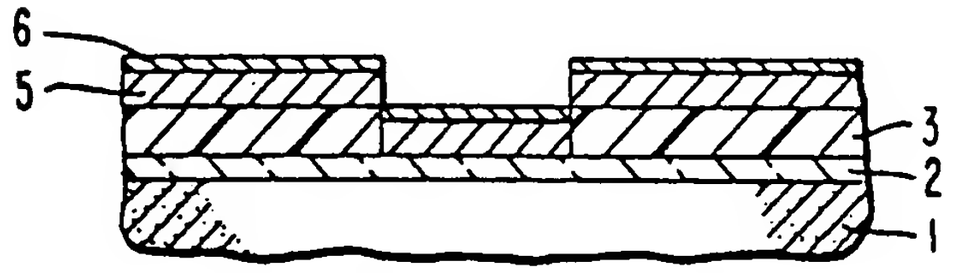

FIG. 1C

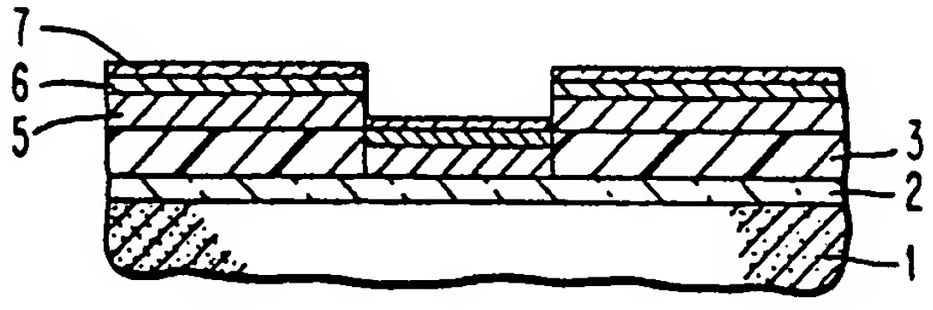

FIG. 1D

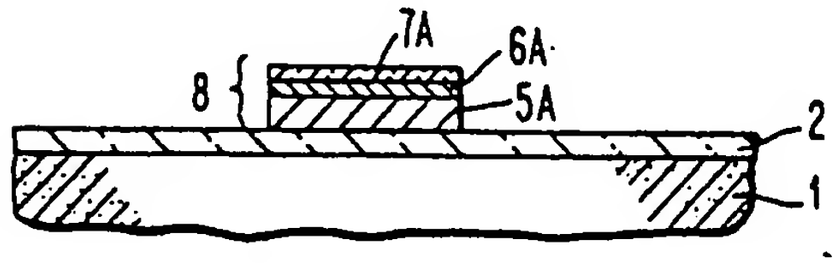

FIG. 1E

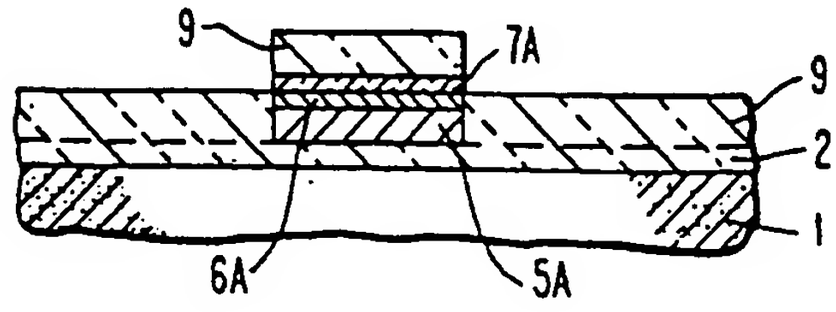

FIG. 1F

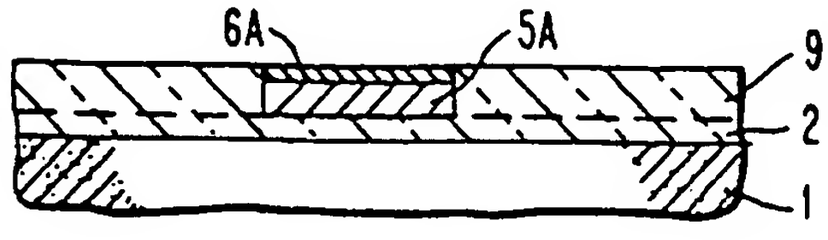

FIG. 1G

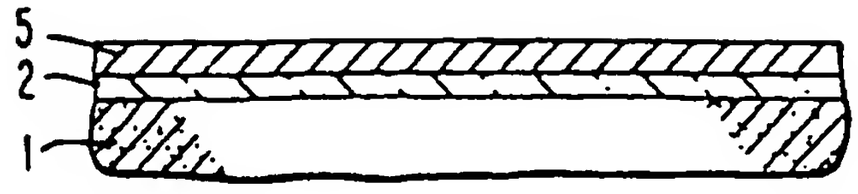

FIG. 2A

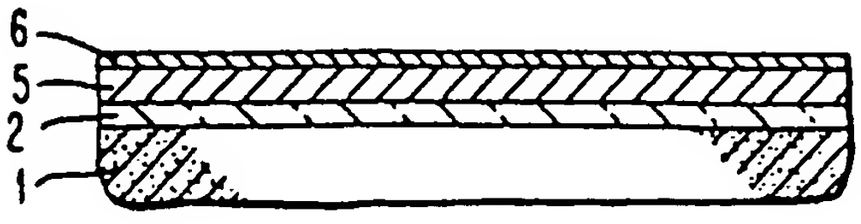

FIG. 2B

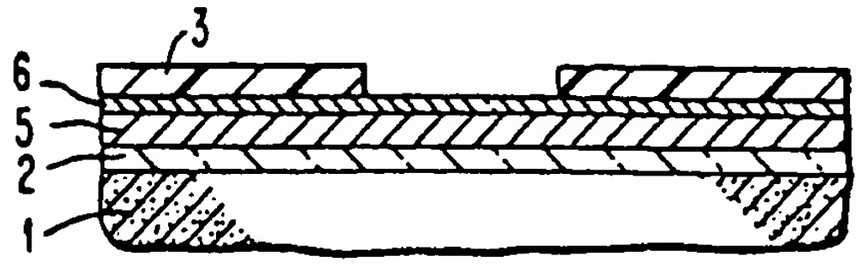

FIG. 2C

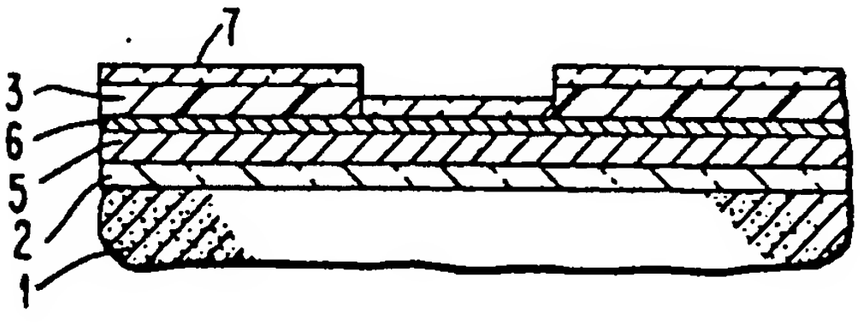

FIG. 2D

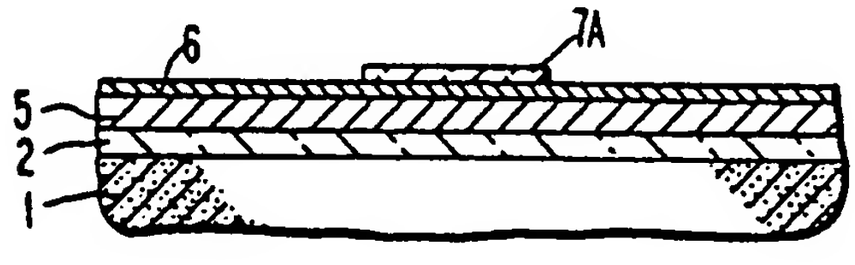

FIG. 2E

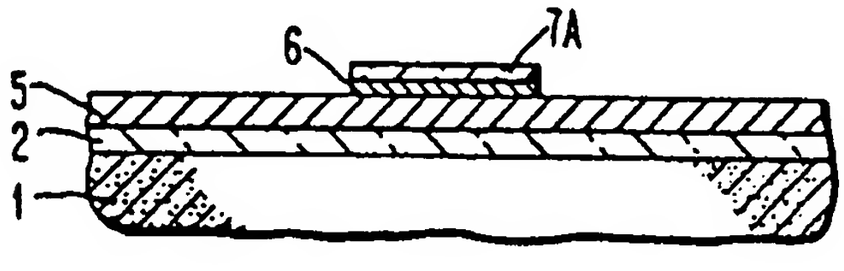

FIG. 2F

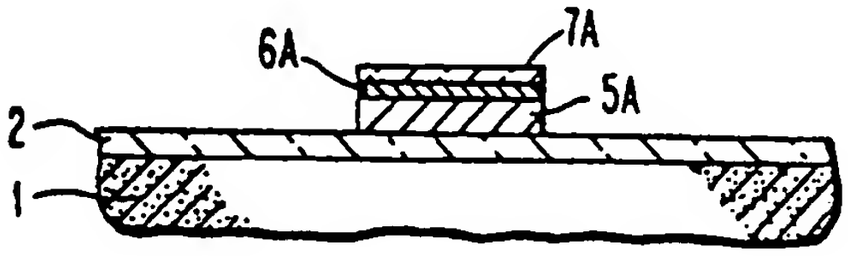

FIG. 2G

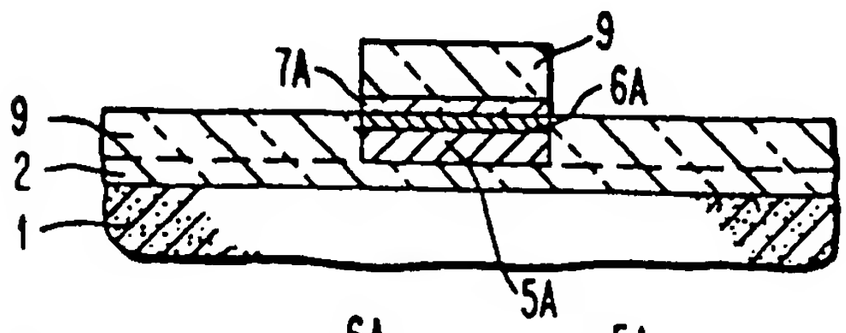

FIG. 2H

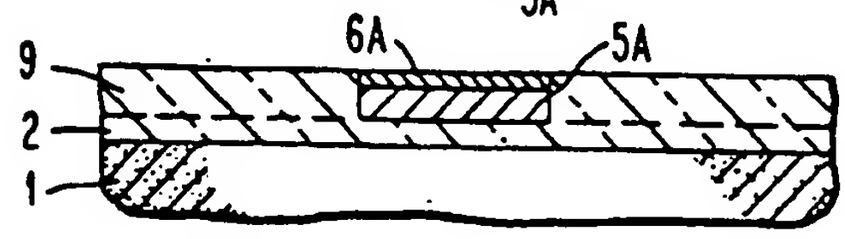

FIG. 2I

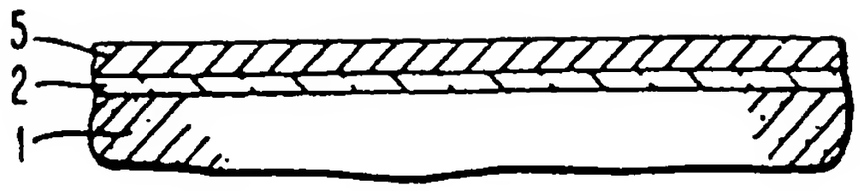

FIG. 3A

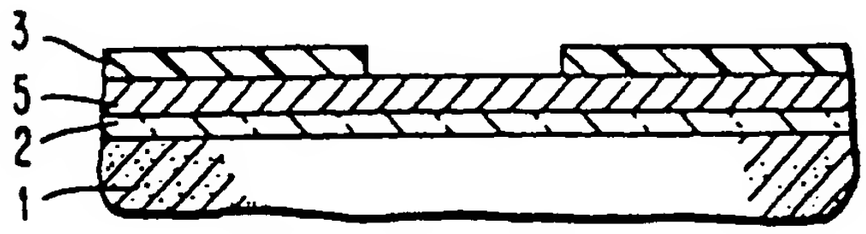

FIG. 3B

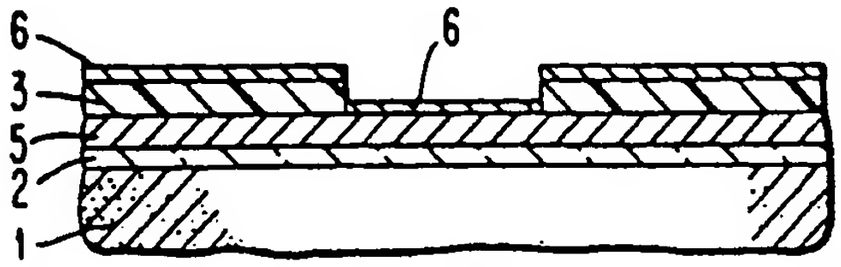

FIG. 3C

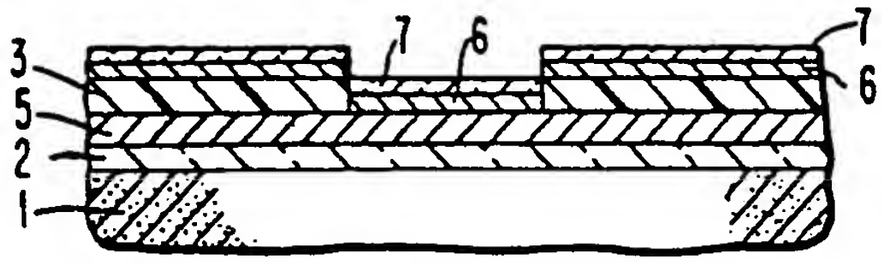

FIG. 3D

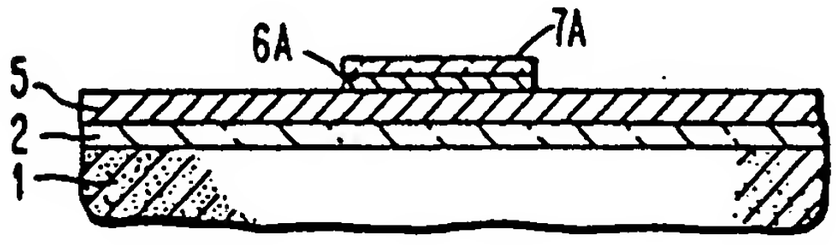

FIG. 3E

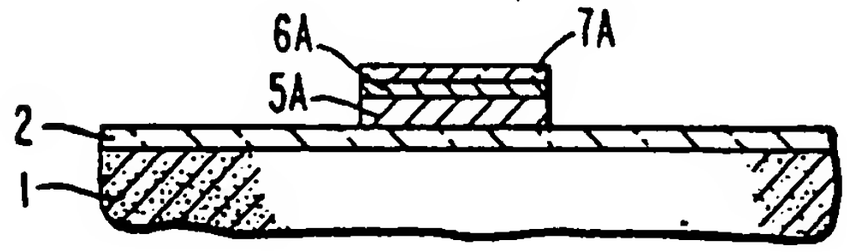

FIG. 3F

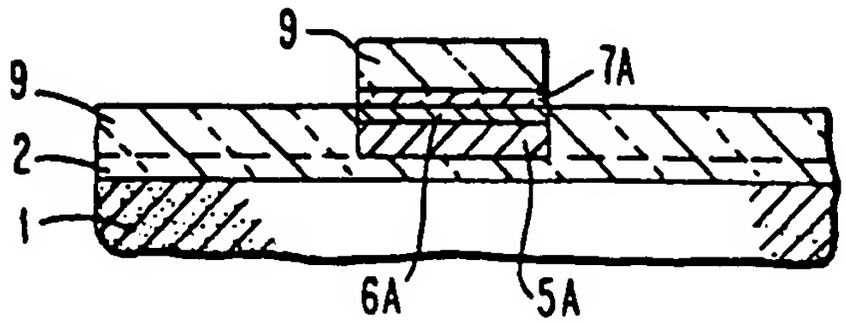

FIG. 3G

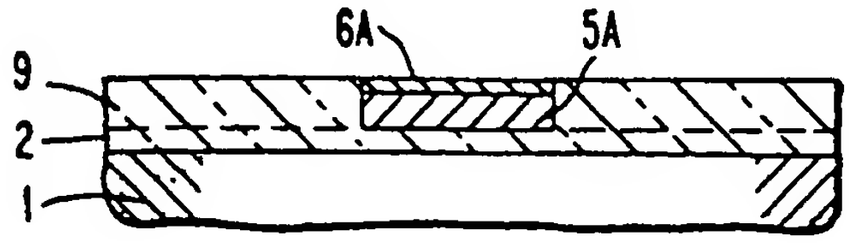

FIG. 3H

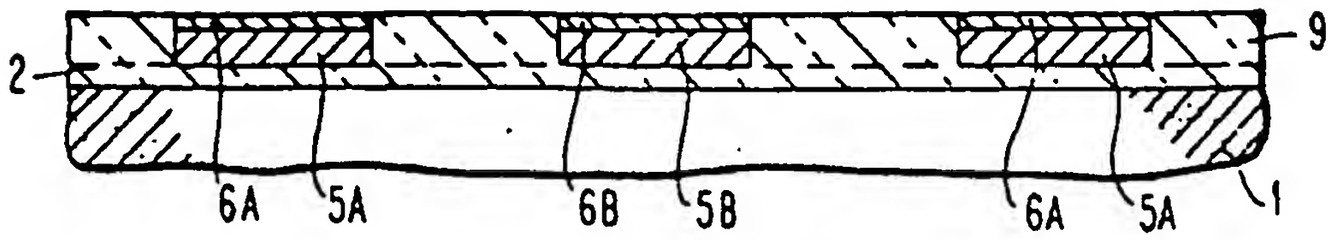

FIG. 4A

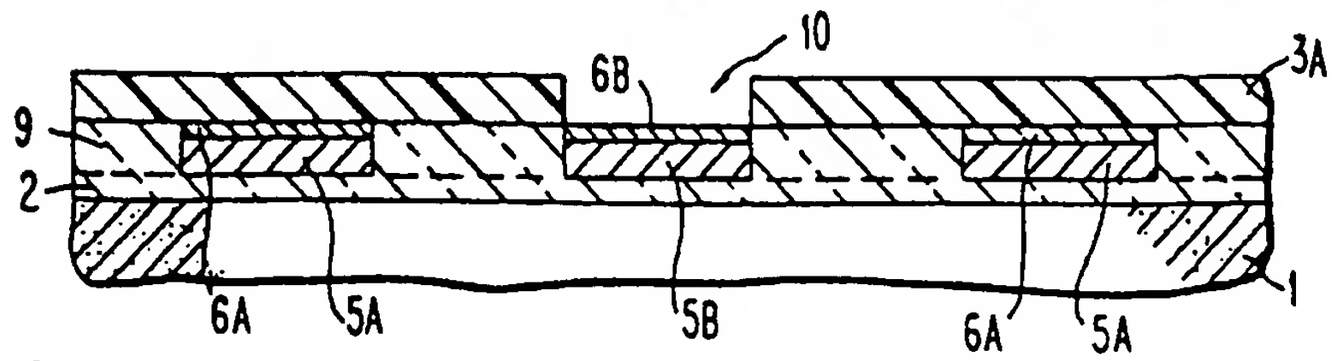

FIG. 4B

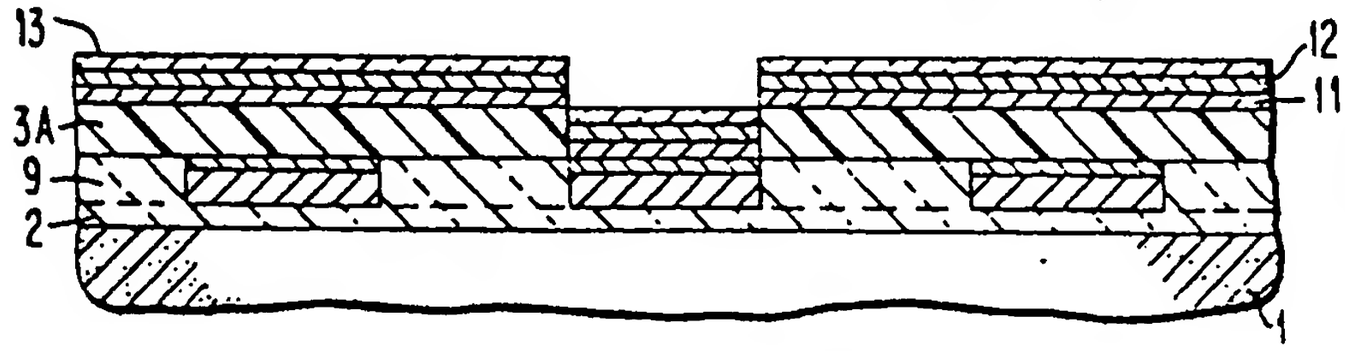

FIG. 4C

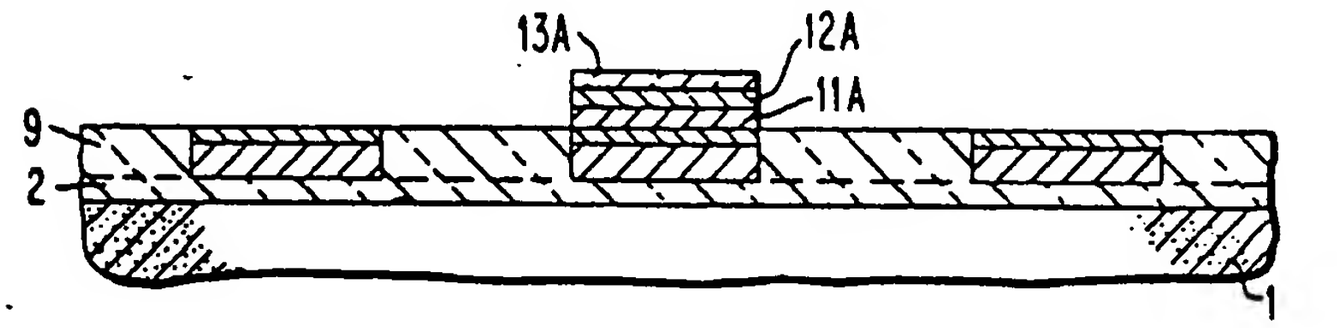

FIG. 4D

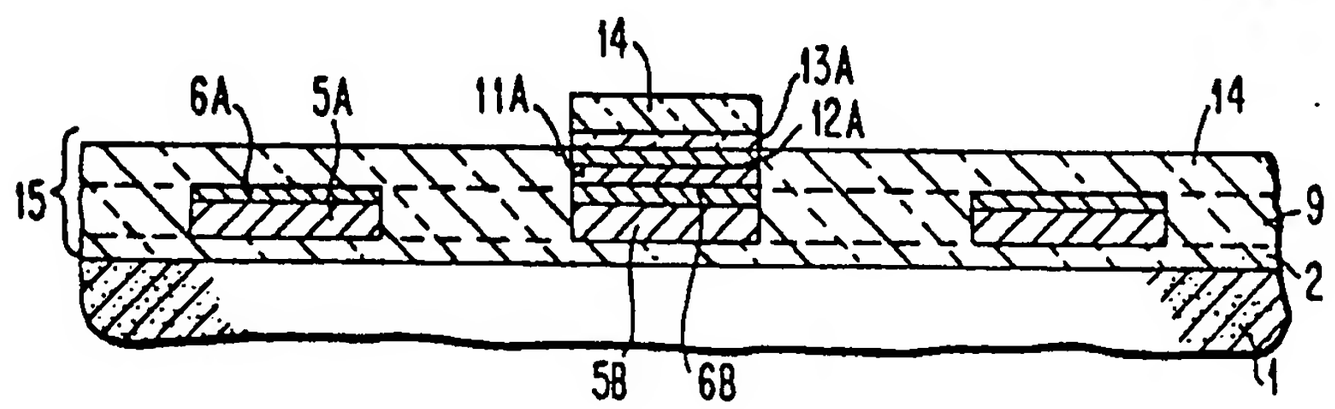

FIG. 4E

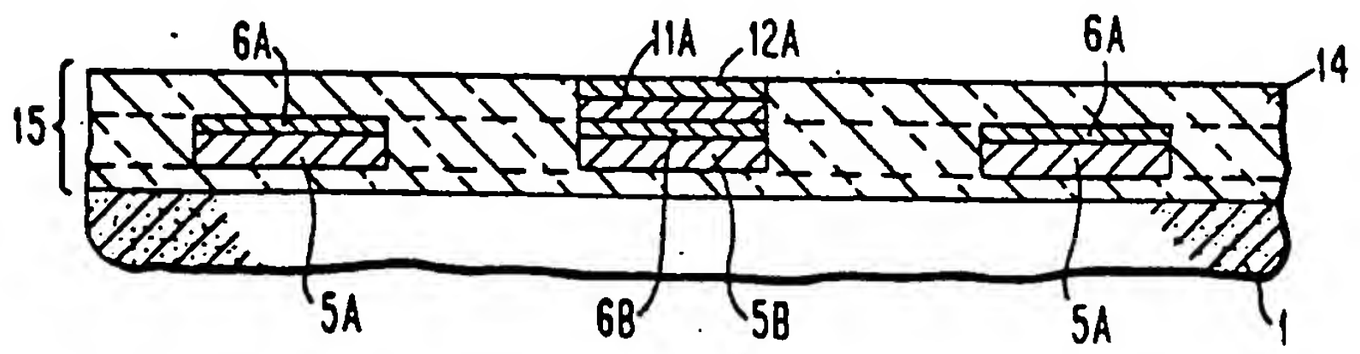

FIG. 4F

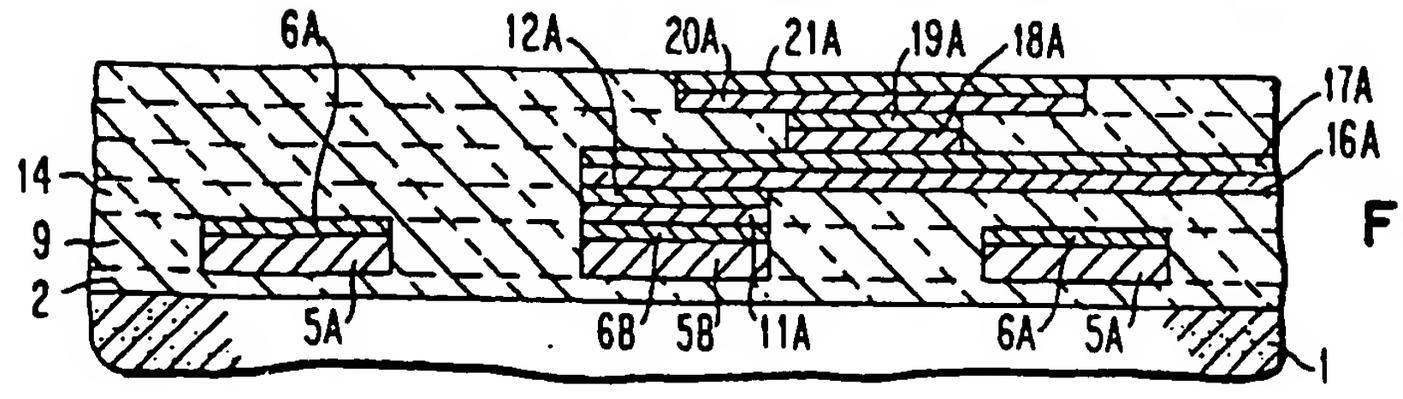

FIG. 4G